



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,740	01/27/2004	Aadu Mirme	23,392-85	1097
23452	7590	12/13/2005	EXAMINER	
PATENT DEPARTMENT LARKIN, HOFFMAN, DALY & LINDGREN, LTD. 1500 WELLS FARGO PLAZA 7900 XERXES AVENUE SOUTH BLOOMINGTON, MN 55431			KRAMSKAYA, MARINA	
		ART UNIT		PAPER NUMBER
				2858
DATE MAILED: 12/13/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

J

Office Action Summary	Application No.	Applicant(s)
	10/765,740	MIRME, AADU
	Examiner	Art Unit
	Marina Kramskaya	2858

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 September 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-16 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-16 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 27 January 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>10/31/2005</u> .	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Election/Restrictions

1. Claims 17-61 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 09/30/2005, and claims 17-61 have been canceled in the communication filed on 09/30/2005.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 & 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Smedley, US 5,278,490.

As per Claim 1, Smedley discloses a reset circuit for an integrating amplifier, including:

first comparator circuitry (20) having a first input terminal (19), a second input terminal (13) and a first output terminal (21);

a first conductive path (19) adapted to couple the first input terminal (19) to a feedback loop (feedback loop of 18) of an integrating amplifier (17) between an

integrator output (19) of the integrating amplifier (17) and an integrating capacitor (see capacitor in FIG. 1) along the feedback loop, whereby a comparator input voltage (V_{int}) at the first input terminal (19) is changed in a predetermined first direction (negative direction: column 6, lines 53-54) and in proportion to an amplitude of an incoming current during integration of the incoming current (column 5, lines 12-16);

a substantially stable voltage source (V_{ref}) for biasing the second input terminal (13) at a first threshold voltage level (V_{ref}) selected to determine one end of an operating range for integration (column 5, lines 41-43), wherein the first comparator input voltage (input at 19), when in said range and when so changed during integration, approaches the first threshold voltage level (V_{ref}); and

a second conductive path (21) coupling (coupling through 22) the first output terminal (21) to the feedback loop (feedback loop of 18);

wherein the first comparator circuitry (20) is adapted, in response to detecting movement of the comparator input voltage out of the operating range beyond the first threshold voltage level (V_{ref}), to generate a predetermined first comparator output voltage level at the first output terminal and to apply the comparator output voltage level to the feedback loop via the second conductive path, thereby to drive the comparator input voltage in a second direction (positive direction: column 6, line 67 - column 7, line 1) opposite said first direction to a point within the operating range for further integration of the incoming current (column 6, line 67 - column 7, line 1).

As per Claim 2, Smedley further discloses a circuit wherein:

the first comparator (20) circuitry further is adapted to stop (go into OFF state) the application of the first comparator output voltage level to the feedback loop (by output 21 to flip flop 22), responsive to detecting movement of the comparator input voltage (V_{int}), during said application, in the second direction beyond the first threshold voltage (V_{ref}) level and into the operating range (column 6, line 67-68).

As per Claim 5, Smedley further discloses a circuit wherein:

the comparator input voltage, when in the operating range, is higher than the first threshold voltage level, and is reduced during integration of the incoming current (column 6, lines 25-28).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3-4 & 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley, US 5,278,490, in view of Nguyen, US 6,519,167.

As per Claim 3, Smedley discloses the reset circuit as applied to Claim 1, above.

Smedley does not disclose an RC network along the first conductive path for interposing a time delay between a given change in the integrator output the voltage and a corresponding change in the comparator input voltage at the first input terminal.

Nguyen discloses a reset circuit including an RC network (R_E and C_i) along the first conductive path (the **+terminal path of U2**) for interposing a time delay between a given change in the integrator (integrator: **U1**) output the voltage (V_i) and a corresponding change in the comparator input voltage (V_i) at the first input terminal (the **+terminal path of U2**).

Therefore, it would have been obvious to a person of ordinary skill in the art to include an RC network, as taught by Nguyen, in the circuit of Smedley, in order to assist in zero crossing detection (Nguyen: column 3, lines 58-62).

As per Claim 4, Smedley discloses the reset circuit as applied to Claim 1, above.

Smedley does not disclose

a second comparator circuitry having a third input terminal, a fourth input terminal and a second output terminal, wherein the third input terminal is coupled to receive the comparator input voltage;

a substantially stable second voltage source for biasing the fourth input terminal at a second threshold voltage level selected to determine a second and opposite end of the operating range, wherein the comparator input voltage, when in the operating range and when driven in said opposite direction, moves toward the second threshold voltage level; and

a third conductive path adapted to couple the second output terminal to the feedback loop;

wherein the second comparator circuitry is adapted, in response to detecting movement of the comparator input voltage in the second direction out of the operating range beyond the second threshold voltage level, to generate a predetermined second comparator output voltage level at the second output terminal and to apply the second comparator output voltage level to the feedback loop via the third conductive path, thereby to drive the comparator input voltage in the first direction to a point within the operating range for further integration of the incoming current.

Nguyen discloses a reset circuitry for an integrating amplifier including:
a second comparator circuitry (U3) having a third input terminal (+ terminal), a fourth input terminal (- terminal) and a second output terminal (output coupled to FF1), wherein the third input terminal is coupled to receive the comparator input voltage (V_{RAMP});

a substantially stable second voltage source (V_{REF}) for biasing the fourth input terminal (- terminal) at a second threshold voltage level (V_{REF}) selected to determine a second and opposite end of the operating range ($-V_{REF}$), wherein the comparator input voltage, when in the operating range and when driven in said opposite direction, moves toward the second threshold voltage level ($-V_{REF}$); and

a third conductive path (output of U3) adapted to couple the second output terminal to the feedback loop (coupled through FF1 back to the feedback of U1);

wherein the second comparator circuitry is adapted, in response to detecting movement of the comparator input voltage in the second direction out of the operating range beyond the second threshold voltage level, to generate a predetermined second comparator output voltage level at the second output terminal and to apply the second comparator output voltage level to the feedback loop via the third conductive path, thereby to drive the comparator input voltage in the first direction to a point within the operating range for further integration of the incoming current (column 4, lines 51-53, 59-62).

Therefore, it would have been obvious to a person of ordinary skill in the art to implement a second comparator circuitry, as taught by Nguyen, in the circuitry of Smedley, in order to compare the feedback voltage of the integrator to a second reference voltage.

As per Claim 12, Smedley, as modified, discloses the circuit as applied to Claim 4, above. Smedley further discloses the comparator input voltage, when in the operating range, is higher than the first threshold voltage level (see V_{int} graph in FIG. 2).

Smedley does not disclose the comparator input voltage, when in the operating range, is lower than the second threshold voltage level, and is reduced during integration of the incoming current.

Nguyen discloses the comparator input voltage, when in the operating range, is lower than the second threshold voltage level (see V_i graph in FIG. 2), and is reduced during integration of the incoming current (see V_i graph in FIG. 2).

Therefore, it would have been obvious to a person of ordinary skill in the art to have the comparator input voltage, when in the operating range, be lower than the second threshold voltage level, and to be reduced during integration of the incoming current, as taught by Nguyen, in the circuit of Smedley, in order to reduce error (Nguyen: column 2, lines 54-59).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley, US 5,278,490, in view of Lai et al., US 5,617,306.

Smedley discloses the circuit as applied to Claim 5, above.

Smedley does not explicitly disclose the substantially stable first comparator output voltage level being a high voltage selected to rapidly charge the integrating capacitor.

Lai discloses a substantially stable first comparator output voltage level (the output of the comparator 16 produces the high voltage V_p : 30) being a high voltage selected to rapidly charge the integrating capacitor (75: C₁) (column 6, lines 61-62).

Therefore, it would have been obvious to a person of ordinary skill in the art to charge the integrating capacitor using the output voltage from the comparator, as taught by Lai, in the circuit of Smedley, in order to adjust the gain of the amplifier.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley in view of Lai et al., as applied to claim 6 above, and further in view of Hwang, US 5,565,761.

Smedley, as modified, discloses the circuit as applied to Claim 6, above.

Smedley does not disclose having a first comparator circuitry adapted to alternatively generate a high voltage and a substantially stable low voltage, wherein applying the first comparator output voltage to the feedback loop consists essentially of switching from the low voltage to the high voltage, and stopping the application to the feedback loop consists essentially of switching from the high voltage to the low voltage.

Hwang discloses

a first comparator circuitry that is adapted to alternatively generate said high voltage and a substantially stable low voltage, wherein applying the first comparator output voltage to the feedback loop consists essentially of switching from the low voltage to the high voltage, and stopping the application to the feedback loop consists essentially of switching from the high voltage to the low voltage (column 3, lines 60-65).

Therefore, it would have been obvious to a person of ordinary skill in the art to have a comparator circuitry to switch from high voltage to low voltage, as taught by Hwang, in the circuit of Smedley, in order to turn off the feedback loop when a reference voltage is reached (Hwang: column 4, lines 27-30).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley in view of Lai et al., as applied to Claim 6 is above, and further in view of Hwang, US 5,742,151.

Smedley, as modified, discloses the circuit as applied to Claim 6, above.

Smedley does not disclose a diode along the second conductive path, oriented with its forward direction coincident with current flow from the first output terminal to the feedback loop.

Hwang discloses a diode (D1) along the second conductive path, oriented with its forward direction coincident with current flow from the first output terminal to the feedback loop (column 8, lines 20-34).

Therefore, it would have been obvious to a person of ordinary skill in the art to use a diode in the feedback loop, as taught by Hwang, in the circuit of Smedley, in order to use the diode current to control the duty cycle of a circuit (Hwang: column 8, lines 20-34).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley, US 5,278,490, in view of Nguyen, US 6,519,167, as applied to claim 12 above, and further in view of Lai et al., US 5,617,306.

As per Claim 13, Smedley, as modified, discloses the circuit as applied to Claim 12, above.

Smedley does not disclose a first comparator circuitry that is adapted to alternatively generate a substantially stable high voltage and a substantially stable low voltage at the first output terminal, and generating the first comparator output voltage level consists essentially of switching from the low voltage to the high voltage to rapidly charge the integrating capacitor.

Lai disclose a first comparator circuitry (CMP: 16) that is adapted to alternatively generate a substantially stable high voltage and a substantially stable low voltage at the first output terminal, and generating the first comparator output voltage level consists essentially of switching from the low voltage to the high voltage to rapidly charge the integrating capacitor (i.e. the switch 13 charges and discharges the integrating capacitor C_I, the voltage V_p is a high voltage that is switched).

Therefore, it would have been obvious to a person of ordinary skill in the art to include a switching from high to low voltage to rapidly charge and discharge an integrating capacitor, as taught by Lai, in the circuit of Smedley, in order to provide a faster reset time (Lai: column 2, lines 36-44).

Allowable Subject Matter

10. Claims 8, 10-11, and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As per Claim 8, the prior art fails to anticipate or make obvious a circuit including: power control circuitry having a fifth input terminal coupled to the first output terminal, a third output terminal, and a fourth conductive path adapted to couple the third output terminal to an input of the integrating amplifier to provide power to the integrating amplifier;

wherein the power control circuitry is adapted to generate a substantially stable high voltage during integration, and to switch from the high voltage to a substantially stable low voltage in response to receiving the high voltage from first comparator circuitry, thereby to shut off power to the integrating amplifier.

As per Claim 10, the prior art fails to anticipate or make obvious a circuit including a limiting circuitry in particular coupled to the second conductive path to prevent excess charging of the integrating capacitor.

Claim 11 further depends from claim 10, and is therefore allowable over prior art.

As per Claim 14, the prior art fails to anticipate or make obvious a circuit characterized in the addition of a second comparator circuitry that is adapted to alternatively generate a substantially stable high voltage and a substantially stable low voltage at the second output terminal, and generating the second comparator output level consists essentially of switching from the high voltage to the low voltage to rapidly discharge the integrating capacitor.

Claims 15 and 16 further depend from claim 14, and are therefore allowable over prior art.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Batarseh et al., US 6,628,106, discloses a reset circuitry with an integrator and two comparators with a feedback loop. Asanuma et al., US 6,963,190, discloses a reset circuit with an integrating amplifier, an integrating capacitor along with a switching means for charging and recharging the capacitor, and a comparator. Athari et al., US 6,781,352, discloses a reset circuitry with an integrator, a reset amplifier, and a comparator connected in a feedback loop.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diane Lee can be reached on (571)272-2399. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Marina Kramskaya
Examiner
Art Unit 2858

M. Kramskaya

MK

V. Nguyen

VINCENT Q. NGUYEN
PRIMARY EXAMINER